

FHG_USB2_OTGDRD



Embedded USB 2.0 OTG High-/Full-/Low-Speed Dual-Role Core

Key Features

The *FHG_USB2_OTGDRD* is a scalable, high performance IP-Module for usage in ASIC- and FPGA- designs to integrate high/full/low-speed USB 2.0 device and host functionality in an embedded system. It provides an ease of use programming interface for the usage of almost every 16/32 bit microcontroller or DSP. The core supports direct RAM access as well as several DMA modes for data exchange with the main memory.

The *FHG_USB2_OTGDRD* supports up to 32 pipes. Every of these data pipes can be configured with a fix address/endpoint and transfer parameters. If more data pipes are required, these assignments may be reconfigured during operation. Therefore, the real number of available pipes can be much larger than the number of hardware pipes using a corresponding software.

- Fully compliant to USB Specification 2.0 and the On-The-Go Supplement, Revision 1.0
- Fully compliant to UTMI Specification 1.05 and UTMI+ Specification 1.0 up to UTMI+ level 2
- Fully compliant to UTMI+ Low Pin Interface Specification 1.0
- High-/Full-Speed device and host capability(480Mbps/12Mbps), host supports Low-Speed devices connected behind High-Speed hubs
- 60 MHz (for 8 bit UTM interface) or 30 MHz (for 16 bit UTM interface) system clock
- Supports OTG Host Negotiation Protocol (HNP)
- Supports OTG Session Request Protocol (SRP)
- Scalable number of pipes , up to 32 pipes are supported
- Configurable for 16 or 32 bit register and data interface (64 bit in preparation)
- Extended Transaction Manager, enables the realization of systems with a minimum of software overhead
- Supports all transfer types (Control, Interrupt, Isochronous, Bulk)
- Pipe direction, transfer type and FIFO size can be configured during run-time
- Supports hardware based scheduling and enhanced large buffer management
- Automatic retry for corrupted data packets
- Automatic split transaction management
- PCI ready
- AMBA AHB ready (AHB slave interface for configuration, AHB master DMA interface or AHB slave interface with Dual-Port RAM for payload data)
- AHB interface tested with Synopsys Amba Verification Suite
- Alternatively, Dual-Port RAM interface available with scalable memory size
- Suspend/Resume/Remote Wakeup support
- Fully synchronous RTL implementation
- Technology independent
- optimized for Altera Cyclone/CycloneII and Stratix/StratixII FPGA families
- optimized for Xilinx Spartan2/3 and Virtex2/4/5 FPGA families
- optimized for Actel ProAsic/ProAsic+ families
- PCI evaluation module available
- Generic USB Device Software Stack with several class drivers available
- Generic USB Host Software Stack with several class drivers available
- Optional, EHCI , OHCI and UHCI software emulation for host mode available

With the features described above, the *FHG_USB2_OTGDRD* brings an USB interface to your system, which is highly efficient from software's point of view:

- All USB related timing critical features are realized in hardware. Therefore, for normal operation software has only to manage the enumeration process
- Once a pipe or channel is established, the only task of the software is to provide data buffers (entire USB protocol is managed by hardware, including data toggle, retry, polling of periodic pipes, ping protocol, split protocol) This reduces the number and frequency of software interrupts to an minimum.
- The required interrupt latency time does not depend on the timing required by the USB packet level, but on the size of data buffers and pipe bandwidth

Typical USB devices working with the USB 2.0 OTG Dual Role Controller Core are for example hard disk devices, multimedia devices, mobile phones, imaging devices, high speed network or industrial applications which require high bandwidth, low latency data transport.

Licenses

The *FHG_USB2_OTGDRD* core can be purchased using one of the following project based licenses:

- VHDL source code for ASIC designs
- Synopsys Design Ware Component for ASIC designs
- VHDL/Verilog/EDIF Netlist for FPGA designs (all Altera families, all Xilinx families, all Actel families)

Other license models can be discussed upon request. The design kit contains the following parts:

- The IP component, depending on the selected license
- VHDL pre-compiled simulation models
- VHDL/Verilog USB 2.0 compliance test suite
- IP integration guideline
- Synthesis scripts
- Optional: PCI evaluation board

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