FHG_USB_DEV

Embedded USB 2.0 Full-Speed Device Core

Key Features

The *FHG_USB_DEV* is a scalable, high performance IP-Module for usage in ASIC- and FPGA-designs to integrate full-speed USB 2.0 device functionality with SRP (Session Request Protocol) in an embedded system. It provides an ease of use programming interface for the usage of almost every 16/32 bit microcontroller or DSP.

The *FHG_USB_DEV* supports up to 31 pipes. Pipe 0 is reserved to work as bi-directional control pipe. Every other pipe can be configured with an endpoint number and transfer parameters. All transfer modes are supported (control, interrupt, isochronous and bulk transfer).

The key features of the *FHG_USB_DEV* are:

- Fully compliant to USB Specification 2.0 and the On-The-Go Supplement, Revision 1.0
- Full-Speed device capability (12Mbps)
- Supports Session Request Protocol (SRP) defined in the On-The-Go supplement
- Scalable number of pipes (max. 31 pipes)
- Supports all transfer types (Control, Interrupt, Isochronous, Bulk)
- Pipe direction, transfer type and fifo size can be configured during run-time
- Supports enhanced large buffer management
- Automatic retry for corrupted data packets
- Configurable for 16 or 32 bit data interface (64 bit in preparation)
- AMBA AHB ready (AHB slave interface for configuration, AHB master DMA interface with Single-Port RAM for payload data)
- AMBA AHB interface testet with Synopsys Amba Verification Suite
- PCI ready
- Dual-Port RAM interface available with scalable memory size
- Suspend/Resume/Remote Wakeup support
- Technology independent RTL implementation
- optimized for Altera Cyclone/CycloneII and Stratix/StratixII FPGA families
- optimized for Xilinx Spartan2/3 and Virtex2/4/5 FPGA families
- optimized for Actel ProAsic/ProAsic+ families
- PCI evaluation module available
- Generic USB Device Software Stack with several class drivers available

With the features described above, the *FHG_USB_DEV* brings an USB interface to your system, which is highly efficient from software's point of view:

- *All* USB related timing critical features are realized in hardware. Therefore, for normal operation software has only to manage the enumeration process
- Once a pipe or channel is established, the only task of the software is to provide data buffers (entire USB protocol is managed by hardware, including data toggle, retry, polling of periodic pipes) This reduces the number and frequency of software interrupts to an minimum.
- The required interrupt latency time does not depend on the timing required by the USB packet level, but on the size of data buffers and pipe bandwidth

Typical USB devices working with the USB Device Controller are for example hard disk devices, multimedia devices, high speed network or industrial applications.

Licenses

The *FHG_USB_DEV* core can be purchased using one of the following project based licenses:

- VHDL source code for ASIC designs
- Synopsys Design Ware Component for ASIC designs
- VHDL/Verilog/EDIF Netlist for FPGA designs (all Altera families, all Xilinx families, all Actel families)

Other license models can be discussed upon request. The design kit contains the following parts:

- The IP component, depending on the selected license
- VHDL pre-compiled simulation models
- VHDL/Verilog USB 2.0 compliance test suite
- IP integration guideline
- Synthesis scripts
- Optional: PCI evaluation board

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