

# EMSYS\_1394b\_VISION



## Embedded IEEE 1394b Link Layer Core for vision application

### Introduction

The *EMSYS\_1394b\_VISION* is a scalable, high performance IP-Module for usage in ASIC- and FPGA- Designs to integrate an IEEE 1394b Link Layer Controller to an embedded system. It provides an ease of use programming interface for the usage of almost every 8/16/32 bit microcontroller or DSP. The *EMSYS\_1394b\_VISION* is optimized for camera/vision applications.

The key features of the *EMSYS\_1394b\_VISION* are:

- Fully compliant to IEEE 1394b Specification
- Fully compliant to IEEE 1394a Specification
- Fully compliant to IEEE 1394-1995 Specification
- Generic 8/16/32 bit microcontroller interface
- Supports B Phy Interface
- Support of 100, 200, 400 and **800 Mb/s** transfer rates in 1394a, 1394b and bilingual mode
- provides full Link Layer and several Transaction Layer functions
- Supports asynchronous transmit and receive (max. packet size 4096 bytes)
- Supports asynchronous/isochronous transmit/receive through separate hardware channel
- Supports simple high bandwidth hardware interface for isochronous transmit (max. packet size 8192 bytes)
- Supports simple high bandwidth hardware interface for isochronous receive (optional, max. packet size 8192 bytes)
- Supports simple high bandwidth hardware interface for asynchronous transmit (optional, max. packet size 4096 bytes)
- Supports cycle master mode (optional)
- Supports transmit and receive of phy packets
- Performs 32-bit CRC generation and check
- fully synchronous RTL implementation
- Technology independent
- optimized for Xilinx Spartan2/3 and Virtex2/4/5 FPGA families
- optimized for Altera Cyclone/CycloneII and Stratix/StratixII FPGA families
- PCI evaluation module available

- Generic IEEE 1394 Software Library available

The *EMSYS\_1394b\_VISION* is optimized for high bandwidth applications. The asynchronous transmit and receive interface is optimized for area, but supports all necessary Link Layer functionality.

Additionally the *EMSYS\_1394b\_VISION* supports isochronous/asynchronous receive/transmit through its high-bandwidth interface. This external interface is optimized for speed and bandwidth. This interface supports multiple channels and has no packet limit per frame.

So the *EMSYS\_1394b\_VISION* is ideal for audio as well as video streaming applications.

### Licenses

The *EMSYS\_1394b\_VISION* core can be purchased using one of the following project based licenses:

- VHDL source code for ASIC designs
- Synopsys Design Ware Component for ASIC designs
- VHDL/Verilog/EDIF Netlist for FPGA designs

Other license models can be discussed upon request. The design kit contains the following parts:

- The IP component, depending on the selected license
- VHDL pre-compiled simulation models
- VHDL/Verilog 1394 compliant automatic test suite
- IP integration guideline
- Synthesis scripts
- Optional: PCI evaluation board

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